CLAIMS

What is claimed is:

1. A power amplifier comprising:

a first switching device connected between a first supply voltage and a first output node;

a second switching device connected between a second supply voltage and a second output node; and

an inductance coupled between the first and second output nodes.

2. The power amplifier of claim 1, wherein a load is coupled to the second output node.

3. The power amplifier of claim 1, further comprising a first capacitor coupled to the first output node, and a second capacitor coupled to the second output node.

4. The power amplifier of claim 1, further comprising a first capacitor coupled to the first output node.

5. The power amplifier of claim 1, further comprising a first capacitor coupled between the first and second output nodes.

6. The power amplifier of claim 1, wherein the first and second switching devices are driven by signals that repeatedly turn the devices on and off.

7. The power amplifier of claim 6, wherein the first and second switching devices are both cycled on during the same time period, and wherein the first and second switching devices are both cycled off during the same time period.

8. The power amplifier of claim 4, wherein the first capacitor is provided by the input capacitance of a third switching device.

9. The power amplifier of claim 3, wherein the first capacitor is provided by the input capacitance of a third switching device, and wherein the second capacitor is provided by the input capacitance of a fourth switching device.

10. The power amplifier of claim 1, wherein the first and second switching devices are comprised of transistors.

11. The power amplifier of claim 1, wherein the first switching device is comprised of a PMOS transistor, and wherein the second switching device is comprised of an NMOS transistor.

12. The power amplifier of claim 1, further comprising a load coupled across the first and second output nodes.

13. The power amplifier of claim 1, further comprising a transformation network coupled to the first and second output nodes.

14. The power amplifier of claim 13, wherein the transformation network further comprises:

a capacitor coupled to the first output node and a third node;

an inductor coupled to the second output node and the third node; and

a load coupled to the third node.

15. The power amplifier of claim 1, further comprising a preamplifier connected to the power amplifier, the preamplifier further comprising:

a third switching device connected between said first supply voltage and a third node and coupled to the input to the first switching device;

a fourth switching device connected between said second supply voltage and a fourth node and coupled to the input to the second switching device; and

a second inductor coupled between the third and fourth nodes.

16. The power amplifier of claim 1, further comprising one or more inductors coupled between the first output node and a third supply voltage.

17. The power amplifier of claim 1, further comprising one or more inductors coupled between the first output node and a third supply voltage, and one or more inductors coupled between the second output node and a fourth supply voltage.

18. A method of reducing the peak output voltage of an amplifier comprising the steps of:

providing an inductor having first and second terminals;

providing a first switching device connected between the first terminal of the inductor and a first supply voltage;

providing a second switching device connected between the second terminal of the inductor and a second supply voltage;

applying a voltage between the first and second terminals of the inductor during a first portion of a clock cycle by turning on the first and second switching devices; and

turning off the first and second switching devices during a second portion of the clock cycle.

19. The method of claim 18, further comprising the steps of providing a first capacitance connected to the first terminal, providing a second capacitance connected to the second terminal, wherein current from the inductor charges or discharges the first and second capacitances during the second portion of the clock cycle.

20. The method of claim 18, further comprising the step of connecting a load to the first node.

21. The method of claim 18, wherein the load includes a reactive network.

22. The method of claim 18, further comprising the step of driving the first and second switching devices such that the switching devices are turned on and off simultaneously.

23. The method of claim 18, further comprising the step of driving the first and second switching devices by repeatedly turning both devices on and then turning both devices off.

24. The method of claim 18, wherein the switching devices are comprised of transistors.

25. The method of claim 18, further comprising the step of differentially connecting a load to the first and second nodes.

26. The method of claim 18, wherein the load is connected across the first and second nodes.

27. The method of claim 18, further comprising the steps of:

providing a third switching device connected between the gate of the first switching device and a third supply voltage;

providing a fourth switching device connected between the gate of the second switching device and a fourth supply voltage; and

providing a second inductor connected between the gates of the first and second switching devices.

28. A differential power amplifier comprising:

a first amplifier having a first switching device connected between a first supply voltage and a first output node, a second switching device connected between a second supply voltage and a second output node, and an inductance coupled between the first and second output nodes;

a second amplifier having a third switching device connected between a third supply voltage and a third output node, a fourth switching device connected between a

fourth supply voltage and a fourth output node, and an inductance coupled between the third and fourth output nodes; and

wherein the first and second amplifiers are coupled together to drive a load.

29. The differential power amplifier of claim 28, wherein the second and fourth output nodes of the first and second amplifiers are coupled together to drive the load.

30. The differential power amplifier of claim 28, wherein the first, second, third, and fourth output nodes of the first and second amplifiers are coupled together to drive the load.

31. The differential power amplifier of claim 28, further comprising:

a first transformation network connected between the first and second output nodes of the first amplifier and the load, and

a second transformation network connected between the third and fourth output nodes of the second amplifier and the load.

32. The differential power amplifier of claim 28, further comprising:

a first transformation network connected between the second output node of the first amplifier and the load, and

a second transformation network connected between the third output node of the second amplifier and the load.

33. The differential power amplifier of claim 28 further comprising:

an inductor coupled between the first output node and the third output node.

34. The differential power amplifier of claim 28 further comprising:
an inductor coupled between the second output node and the fourth output node.

35. The differential power amplifier of claim 31, wherein the first transformation network further comprises:
a first capacitor coupled to the second output node of the first amplifier and coupled to the load; and
a first inductor coupled to the first output node of the first amplifier and coupled to the load.

36. The differential power amplifier of claim 31, wherein the second transformation network further comprises:
a second capacitor coupled to the third output node of the second amplifier and coupled to the load; and
a second inductor coupled to the fourth output node of the second amplifier and coupled to the load.

37. The differential power amplifier of claim 28, wherein the first amplifier receives first and second inputs.

38. The differential power amplifier of claim 37, wherein the first and second switching devices of the first amplifier are enabled and disabled simultaneously; and
wherein the third and fourth switching devices of the second amplifier are enabled and disabled simultaneously.

39. The differential power amplifier of claim 38, wherein the first and second switching devices of the first amplifier are enabled during the time that the third and fourth switching devices of the second amplifier are disabled, and wherein the third and fourth switching devices of the second amplifier are enabled during the time that the first and second switching devices of the first amplifier are disabled.

40. The differential power amplifier of claim 28, wherein the amplifier further comprises:

a first capacitance coupled between the first output node and the first supply voltage;

a second capacitance coupled between the second output node and the first supply voltage; and

wherein the second amplifier further comprises:

a third capacitance coupled between the third output node and a third supply voltage;

a fourth capacitance coupled between the fourth output node and a fourth supply voltage.

41. The differential power amplifier of claim 40, wherein the first, second, third, and fourth capacitances are provided by capacitors.

42. The differential power amplifier of claim 40 wherein the first, second, third, and fourth capacitances are provided by the input capacitance of fifth, sixth, seventh, and eighth switching devices, respectively.

43. The differential power amplifier of claim 42, wherein the fifth switching device is coupled to the third output node, and the sixth switching device is coupled to the fourth

output node, and the seventh switching device is coupled to the first output node, and the eighth switching device is coupled to the second output node.

44. The differential power amplifier of claim 28, further comprising a preamplifier for each of the first and second power amplifiers.

45. The differential power amplifier of claim 44, wherein each of the preamplifiers further comprise:

fifth and sixth switching devices connected between the first and second supply voltages; and

a third inductor connected between the fifth and sixth switching devices.

46. The differential power amplifier of claim 28, wherein the first and second amplifiers are cross-coupled.